

Appl. No. : 10/724,534
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REMARKS

The April 3, 2007 Office Action was based on pending Claims 1-6, 8-20, 31, 33, 37-40 and 42-44. This amendment amends Claims 1, 12, 31, and 40. New Claims 50 and 51 are added. Thus, Claims 1-6, 8-20, 31, 33, 37-40, 42-44, 50, and 51 are pending and presented for further consideration.

The April 3, 2007 Office Action rejected Claims 1-4, 8, 9, 11-16, 18-20, 31, 33, 37, 39, 40, 43 and 44 as being unpatentable over U.S. Patent No. 5,948,100 to Hsu et al. ("Hsu") in view of U.S. Patent No. 6,000,008 to Simcoe ("Simcoe").

The Office Action further rejected Claims 5 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Hsu and Simcoe, and further in view of U.S. Patent No. 4,860,192 to Sachs et al. ("Sachs").

The Office Action further rejected Claims 10, 17 and 42 under 35 U.S.C. § 103(a) as being unpatentable over Hsu and Simcoe, and further in view of U.S. Patent No. 5,764,946 to Tran et al. ("Tran").

The Office Action further rejected Claim 38 under 35 U.S.C. § 103(a) as being unpatentable over Hsu and Simcoe, and further in view of U.S. Patent No. 6,085,291 to Hicks et al. ("Hicks").

The Applicant notes that the base Claims 1, 12, 31, and 40 are amended to include the further limitations that instructions can be performed out of an original program order as part of a predicted path that has not yet been taken and routing the address of cached data matching a data string is performed after any instructions are performed that modify data within the address. The Applicant respectfully notes that support for these additional limitations may be found for example at paragraph [0041] of the corresponding published application.

New dependent Claims 50 and 51 recite the further limitation that comparing the portions of the data string comprises comparing an entire cache line in a single cycle. The Applicant notes that support for these limitations may be found for example in paragraph [0061] of the corresponding published application.

Appl. No. : 10/724,534
Filed : November 26, 2003

CLAIM REJECTIONS UNDER 35 U.S.C. § 103(a)

The April 3, 2007 Office Action rejected Claims 1-4, 8, 9, 11-16, 18-20, 31, 33, 37, 39, 40, 43, and 44 as being unpatentable over Hsu in view of Simcoe. Claims 5 and 6 were rejected as being unpatentable over Hsu and Simcoe, and further in view of Sachs. Furthermore, Claims 10, 17 and 42 were rejected as being unpatentable over Hsu and Simcoe, and further in view of Tran. Claim 38 was also rejected as being unpatentable over Hsu and Simcoe, and further in view of Hicks.

In view of the foregoing amendments and for at least the reasons set forth below, Applicant respectfully requests reconsideration of the aforementioned claims.

Independent Claim 1

With particular reference to amended Claim 1, an embodiment of Applicant's invention includes a method of searching data for a match with a data string. The method comprises: routing a series of assembly language instructions to a processor having a first execution circuit for executing arithmetic and logic instructions, wherein the instructions can be performed out of an original program order as part of a predicted branch that has not yet been taken; analyzing the series of assembly language instructions to detect an instruction to perform a search operation, the search instruction comprising a data string and a starting address; and routing the search instruction undecoded to a data string manipulation circuit, independent of the first execution circuit, capable of performing string manipulation instructions.

The method also includes, among other things, comparing portions of the data string with consecutive portions of cache memory data; generating a match signal for each portion of the cache memory data that matches a respective data string portion; identifying a plurality of match signals indicating the consecutive portions the cache memory data that together match the data string; and routing an address of cache data matching the data string to the data string manipulation circuit, wherein the routing the address of cached data matching the data string is performed after any instructions are performed that modify data within the address.

Neither Hsu, nor Simcoe, nor a combination thereof teaches or suggests the combination of features recited in the Applicant's method of Claim 1 as currently

amended. More particularly, Hsu and Simcoe fail to disclose routing the address of cached data matching the data string after any instructions are performed that modify data within the address.

Hsu appears to be directed to branch instruction prediction in a superscalar pipelined processor. In particular, Hsu discloses certain methods for predicting a branch address in a sequence of instructions using a branch target buffer (see, for example, Figure 9). The disclosed methods include receiving a search address and simultaneously comparing a tag portion of the search address with tag portions of entries stored in multiple blocks of memory locations in the branch target buffer (see, e.g., col. 13, line 42, through col. 14, line 65).

The Examiner recognizes that Hsu does not teach several of the limitations of Claim 1 (i.e., recited acts of "comparing portions of test data . . .; generating a match signal for each portion . . .; and identifying a plurality of match signals"). Moreover, Hsu does not teach or suggest: (i) routing a series of assembly language instructions to a processor having a first execution circuit for executing arithmetic/logic instructions and a second circuit for performing string manipulation instructions; and (ii) analyzing the series of assembly language instructions to detect and route an undecoded search instruction to the second (data string manipulation) circuit. Rather, Hsu's fetcher 400, which the Office Action identifies as a "data string manipulation circuit," outputs a fetch address (FA) and a search address (SA) based on a series of signals and addresses received from a plurality of components (i.e., decoder unit 120, execution unit 130 and branch target buffer 200).

In addition, Simcoe, which was cited by the Office Action for teaching a plurality of comparators that compare portions of sequential data with consecutive portions of cache memory data, does not teach or suggest the various elements of amended Claim 1 as described above. For instance, Simcoe does not teach or suggest: (i) routing a series of assembly language instructions to a processor having a first execution circuit for executing arithmetic/logic instructions and a second circuit for performing string manipulation instructions; and (ii) analyzing the series of assembly

Appl. No. : 10/724,534
Filed : November 26, 2003

language instructions to detect and route an undecoded search instruction to the second (data string manipulation) circuit.

Because the cited references do not teach each and every element as recited and arranged in amended Claim 1, Applicant respectfully submits that Claim 1 is patentably distinguished over the cited references. Applicant, therefore, respectfully requests the rejection under 35 U.S.C. § 103(a) to be withdrawn.

Independent Claims 12, 31 and 40

Amended independent Claims 12, 31 and 40 are each believed to be patentably distinguished over the cited references for reasons similar to those set forth above with respect to amended independent Claim 1 and for the different aspects recited therein.

Dependent Claims 2-6, 8-11, 13-20, 33, 37-39 and 42-44

Claims 2-6 and 8-11 depend from amended independent Claim 1 and are believed to be patentably distinguished over the cited references for reasons similar to those set forth above with respect to Claim 1 and for the additional features recited therein.

Claims 13-20 depend from amended independent Claim 12 and are believed to be patentably distinguished over the cited references for reasons similar to those set forth above with respect to Claim 1 and for the additional features recited therein.

Claims 33 and 37-39 depend from amended independent Claim 31 and are believed to be patentably distinguished over the cited references for the reasons similar to those set forth above with respect to Claim 1 and for the additional features recited therein.

Claims 42-44 depend from amended independent Claim 40 and are believed to be patentably distinguished over the cited references for the reasons similar to those set forth above with respect to Claim 1 and for the additional features recited therein.

Dependent Claims 5, 6, 10, 17, 38, and 42

The April 3, 2007 Office Action also rejects Claims 5, 6, 10, 17, 38, and 42 under 35 U.S.C. § 103(a) as unpatentable over Hsu in view of Simcoe and further in view of Sachs, Tran, or Hicks. The Applicant has reviewed the Sachs, Tran, and Hicks

Appl. No. : 10/724,534
Filed : November 26, 2003

references and respectfully asserts that the combination of references fails to disclose or suggest the combination of features recited in the base claims 1, 12, 31, and 40. The Applicant believes that Claims 5, 6, 10, 17, 38, and 42 properly further define the Applicant's claimed invention and are patentable due at least in part to their dependence on the respective base claim. The Applicant thus respectfully requests that the rejection under 35 U.S.C. § 103(a) to be withdrawn.

New Claims 50 and 51

The Applicant believes that new Claims 50 and 51 properly further define the Applicant's claimed invention and are patentable due at least in part to their dependence on the respective base claim. The Applicant respectfully requests prompt allowance of the new claims.

Information About Other Cases

In addition to the Amendments and Remarks provided above, Applicant provides the following table to aid the Examiner during prosecution. The following U.S. issued patents and patent applications are related to the above-captioned application in that they have at least one listed inventor or assignee in common with the above-captioned application:

UNITED STATES ISSUED PATENTS/PENDING APPLICATIONS

Patent No./ App. No.	Title	Attorney Docket No.
6658552	Processing System With Separate General Purpose Execution Unit And Data String Manipulation Unit	MTIPAT.024A
7093093	Cache Management System	MTIPAT.024DV1
7120744	System and Method For Managing a Cache Memory	MTIPAT.024DV2
7103719	System and Method For Managing a Cache Memory	MTIPAT.024DV3
7165143	System and Method For Managing a Cache Memory	MTIPAT.024DV5
10/705423	Processing System With General Purpose Execution Unit and Separate Independently Operating Data String Manipulation Unit	MTIPAT.024C1

Copies of the patents, applications, and pending claims, including any office actions and allowances, are available through PAIR. However, if the Examiner so requests, Applicant will be happy to provide the Examiner with copies of any patents, applications, pending claims, office actions, allowances, or any other documents, at any time.

Appl. No. : **10/724,534**
Filed : **November 26, 2003**

Further, Applicant notes for the record that the claims of the present application are different and may be broader in scope than the claims in any related patent or application. To the extent that any statements made in a related case (such as amendments or characterizations regarding the scope of a claim or prior art) could be construed as a disclaimer of any subject matter supported by the present disclosure, Applicant rescinds and retracts such disclaimer. Accordingly, any listed or referenced prior art may need to be re-visited. Further, any objections or rejections made by the Examiner in the issued and allowed cases identified above may need to be re-visited.

Claims canceled in this application are done so without prejudice. Moreover, although the present communication may include alterations to the application or claims, Applicant is not conceding that the previously pending claims are not patentable over the art of record. Rather, any alterations or characterizations are being made to facilitate expeditious prosecution of this application. Applicant reserve the right to later pursue any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that the Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Appl. No. : 10/724,534
Filed : November 26, 2003

SUMMARY

Although amendments and cancellations have been made, no acquiescence or estoppel is or should be implied thereby. Rather, the amendments and cancellations are made only to expedite prosecution of the present application, and without prejudice to presentation or assertion, in the future, of claims on the subject matter affected thereby. Furthermore, any arguments in support of patentability and based on a portion of a claim should not be taken as founding patentability solely on the portion in question; rather, it is the combination of features or acts recited in a claim which distinguishes it over the prior art.

In view of the foregoing, the present application is believed to be in condition for allowance, and such allowance is respectfully requested. If further issues remain to be resolved, the Examiner is cordially invited to contact the undersigned such that any remaining issues may be promptly resolved. Also, please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

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